WHAT IS CLAIMED IS:

1. A method of fabricating a CMOS device in which p- and n-type thin film transistors are formed, comprising the steps of:

non-selectively doping the whole of a thin film with p-type impurities, said thin film to be an active semiconductor layer including prospective regions to form said p- and n-type thin film transistors;

selectively doping only the prospective region to form said n-type thin film transistor with p-type impurities at a higher concentration than that in said step of non-selectively doping; and

annealing said thin film to activate the p-type impurities contained therein,

wherein threshold voltages of said p- and n-type thin film transistors are independently set by said step of non-selectively doping and said step of selectively doping.

2. A method according to claim 1, wherein

said step of non-selectively doping is performed such that said thin film has a concentration distribution of p-type impurities substantially uniform in a direction of thickness of said thin film, and

said step of selectively doping is performed such that said thin film has a concentration distribution of p-type impurities with a peak near a surface in

the direction of thickness of said thin film.

3. A method according to claim 1, wherein

said step of non-selectively doping is performed such that said thin film has a concentration distribution of p-type impurities substantially changing broadly in a direction of thickness of said thin film, and

said step of selectively doping is performed such that said thin film has a concentration distribution of p-type impurities with a peak near a surface in the direction of thickness of said thin film.

4. A method according to claim 1, wherein

said step of non-selectively doping is performed by one of processes selected from gas addition and ion-doping when said thin film is formed, and

said step of selectively doping is performed by an ion-doping process.

5. A method according to claim 4, wherein said ion-doping process is performed by using a non-mass separation type ion-doping apparatus having a DC filament ion source.

6. A method according to claim 1, wherein the concentration of p-type impurities in said thin film is adjusted to not more than $1 \times 10^{18}/cm^3$ by said step of non-selectively doping.

7. A method according to claim 4, wherein the dose of said ion-doping process in said step of non-selectively doping is within the range of $1 \times 10^{11}/cm^2$

to 1 x $10^{13}/cm^2$.

8. A method according to claim 4, wherein the gas amount of said gas addition process in said non-selectively doping is within the range of 1 to 10 ppm.

9. A method according to claim 1, wherein said thin film is an amorphous silicon film,

said method comprises a step of crystallizing said amorphous silicon film by irradiation with a laser beam to form a polysilicon film, after said step of non-selectively doping, and

said step of selectively doping is performed for said polysilicon film.

10. A method according to claim 1, wherein said method further comprises a step of crystallizing an amorphous silicon film by irradiation with a laser beam to form a polysilicon film, and

said step of non-selectively doping is performed by using said polysilicon film as said thin film.

11. A method according to claim 1, further comprising a step of separating said thin film into islands of said prospective regions to form said p- and n-type thin film transistors, after said step of selectively doping.

12. A method according to claim 1, wherein said method further comprises a step of separating said thin film into islands of said prospective regions to form said p- and n-type thin film transistors, after said step of non-selectively doping, and

said step of selectively doping is performed after said step of separating.

13. A method according to claim 12, wherein said method further comprises a step of forming a gate insulating film on said islands of said prospective regions and successively forming gate electrode patterns on said gate insulating film, and

said step of selectively doping is performed on condition that p-type impurities penetrate said gate electrode patterns and said gate insulating film and stop in portions of said islands regions immediately below said gate electrode patterns.

14. A method according to claim 4, wherein said method further comprises the steps of:

forming a gate electrode pattern, and

forming a gate insulating film so as to cover said gate electrode pattern, and

said thin film is formed on said gate insulating film and, after then, said step of non-selectively doping and said step of selectively doping are performed.

15. A method according to claim 12, wherein said method comprises:

a step of forming gate insulating film patterns and gate electrode patterns on said islands separated from said thin film after said step of non-selectively doping, such that said islands, said gate insulating film patterns, and said gate electrode

patterns narrow down in this order;

said step of selectively doping in the state that only the island to be n-type is exposed, on condition that p-type impurities penetrate the corresponding gate electrode pattern and gate insulating film pattern and stop in a portion of said island immediately below said gate electrode pattern;

a step of performing doping with n-type impurities at a higher concentration than that in said step of selectively doping, in the state that only said island to be n-type is exposed, on condition that n-type impurities penetrate exposed portions of said gate insulating film pattern and stop in portions of said island region corresponding to said exposed portions of said gate insulating film pattern and further performing doping with n-type impurities at a still higher concentration such that n-type impurities stop in exposed portions of said island; and

a step of doping with p-type impurities at a higher concentration than that in said step of selectively doping, in the state that only the island to be p-type is exposed, such that p-type impurities penetrate exposed portions of the corresponding gate insulating film pattern and stop in portions of said island corresponding to said exposed portions of said gate insulating film pattern and further doping with p-type impurities at a still higher concentration

such that p-type impurities stop in exposed portions of said island.

16. A method according to claim 12, wherein said method comprises:

a step of forming gate insulating film patterns and gate electrode patterns on said islands separated from said thin film after said step of non-selectively doping, such that said islands, said gate insulating film patterns, and said gate electrode patterns narrow down in this order;

a step of doping the whole of said islands, said gate insulating film patterns and said gate electrode patterns with p-type impurities at a higher concentration than that in said step of selectively doping, on condition that p-type impurities penetrate exposed portions of said gate insulating film patterns and stop in portions of said islands corresponding to said exposed portions of said gate insulating film patterns and further doping said whole with p-type impurities at a still higher concentration such that p-type impurities stop in exposed portions of said islands;

said step of selectively doping in the state only the island to be n-type is exposed, on condition that p-type impurities penetrate the corresponding gate electrode pattern, and gate insulating film pattern and stop in portions of said island immediately below said gate electrode pattern; and

a step of doping with n-type impurities in the state that only said island to be n-type is exposed, on condition that n-type impurities penetrate exposed portions of the corresponding gate insulating film pattern and stop in portions of said island corresponding to said exposed portions of said gate insulating film pattern, at a concentration at which said portions of said island can become n-type, and further doping with n-type impurities such that n-type impurities stop in exposed portions of said island at a concentration at which said exposed portions of said island can become n-type.

17. A method of fabricating a semiconductor device including a plurality of CMOS transistors each of which comprises p- and n-type thin film transistors and which are classified into at least two element groups having different operating voltages, said method comprising the steps of:

non-selectively doping a thin film with p-type impurities, said thin film to be an active semiconductor layer including first prospective regions to form p-type thin film transistors and second prospective regions to form n-type thin film transistors;

selectively doping only said second prospective regions of said thin film with p-type impurities at a higher concentration than that in said step of non-selectively doping; and

annealing said thin film to activate the p-type impurities contained therein,

wherein each of said element groups is subjected to a predetermined number of times of said step of non-selectively doping necessary for the element group and a predetermined number of times of said step of selectively doping necessary for the element group so that threshold voltages of the p- and n-type thin film transistors constituting the element group are independently set in accordance with the operating voltage of the element group.

18. A method of fabricating a semiconductor device including a plurality of CMOS transistors each of which comprises p- and n-type thin film transistors and which are classified into at least two element groups having different operating voltages, said method comprising the steps of:

non-selectively doping a thin film with p-type impurities, said thin film to be an active semiconductor layer including first prospective regions to form p-type thin film transistors and second prospective regions to form n-type thin film transistors;

selectively doping only said second prospective regions of said thin film with p-type impurities at a higher concentration than that in said step of non-selectively doping; and

annealing said thin film to activate the p-type

impurities contained therein,

wherein each of part of said element groups is subjected to a predetermined number of times of said step of non-selectively doping necessary for the element group and a predetermined number of times of said step of selectively doping necessary for the element group, and each of the other part of said element groups is subjected to only a predetermined number of times of said step of non-selectively doping necessary for the element group, so that threshold voltages of the p- and n-type thin film transistors constituting each of said element groups are independently set in accordance with the operating voltage of the element group.

19. A method according to claim 17, wherein

said step of non-selectively doping is performed by one of processes selected from gas addition and ion-doping when said thin film is formed, and

said step of selectively doping is performed by an ion-doping process.

20. A method according to claim 19, wherein said ion-doping process is performed by using a non-mass separation type ion-doping apparatus having a DC filament ion source.

21. A method according to claim 17, wherein the concentration of p-type impurities in said thin film is adjusted to not more than $1 \times 10^{18}/cm^3$ by said step of non-selectively doping.

22. A method of manufacturing an image display apparatus including an image display unit with a plurality of pixels arranged in a matrix, a first control circuit for controlling the drive of rows of said image display unit, and a second control circuit for controlling the drive of columns of said image display unit, at least one of said image display unit and said first and second control circuits including CMOS transistors each of which comprises p- and n-type thin film transistors and which have different operating voltages, said method comprising the steps of:

non-selectively doping a thin film with p-type impurities, said thin film to be an active semiconductor layer including first prospective regions to form p-type thin film transistors and second prospective regions to form n-type thin film transistors;

selectively doping only said second prospective regions of said thin film with p-type impurities at a higher concentration than that in said step of non-selectively doping; and

annealing said thin film to activate the p-type impurities contained therein,

wherein each of said CMOS transistors is subjected to a predetermined number of times of said step of non-selectively doping necessary for the CMOS transistor and a predetermined number of times of

said step of selectively doping necessary for the CMOS transistor so that threshold voltages of the p- and n-type thin film transistors constituting the CMOS transistor are independently set in accordance with the operating voltage of the CMOS transistor.

23. A method of manufacturing an image display apparatus including an image display unit with a plurality of pixels arranged in a matrix, a first control circuit for controlling the drive of rows of said image display unit, and a second control circuit for controlling the drive of columns of said image display unit, at least one of said image display unit and said first and second control circuits including CMOS transistors each of which comprises p- and n-type thin film transistors and which have different operating voltages, said method comprising the steps of:

non-selectively doping a thin film with p-type impurities, said thin film to be an active semiconductor layer including first prospective regions to form p-type thin film transistors and second prospective regions to form n-type thin film transistors;

selectively doping only said second prospective regions of said thin film with p-type impurities at a higher concentration than that in said step of non-selectively doping; and

annealing said thin film to activate the p-type

impurities contained therein,

wherein each of part of said CMOS transistors is subjected to a predetermined number of times of said step of non-selectively doping necessary for the CMOS transistor and a predetermined number of times of said step of selectively doping necessary for the CMOS transistor, and each of the other part of said CMOS transistors is subjected to only a predetermined number of times of said step of non-selectively doping necessary for the CMOS transistor, so that threshold voltages of the p- and n-type thin film transistors constituting each of said CMOS transistors are independently set in accordance with the operating voltage of the CMOS transistor.

24. A method according to claim 23, wherein

said image display unit has liquid crystal cells as said pixels and CMOS transistors with a high operating voltage, and

said first control circuit comprises a low-voltage operation unit having CMOS transistors with a relatively low operating voltage and a high-voltage operation unit having CMOS transistors with a high operating voltage.

25. A method according to claim 23, wherein

said step of non-selectively doping is performed by one of processes selected from gas addition and ion-doping when said thin film is formed, and

said step of selectively doping is performed by

an ion-doping process.

26. A method according to claim 25, wherein said ion-doping process is performed by using a non-mass separation type ion-doping apparatus having a DC filament ion source.

27. A method according to claim 23, wherein the concentration of p-type impurities in said thin film is adjusted to not more than 1 x $10^{18}/cm^3$ by said step of non-selectively doping.

28. A CMOS device in which p- and n-type thin film transistors are formed, wherein

said p-type thin film transistor has a first active semiconductor layer formed by doping its channel region with p-type impurities at a concentration of not more than 1 x $10^{18}/cm^3$ such that the concentration distribution in a direction of the thickness of said first active semiconductor layer is substantially uniform, and

said n-type thin film transistor has a second active semiconductor layer formed by doping its channel region with p-type impurities at a higher concentration than that in said first active semiconductor layer such that the concentration distribution in a direction of the thickness of said second active semiconductor layer has a peak near a surface.

29. A CMOS device in which p- and n-type thin film transistors are formed, wherein

said p-type thin film transistor has a first active semiconductor layer formed by doping its channel region with p-type impurities at a concentration of not more than 1 x $10^{18}/cm^3$ such that the concentration distribution in a direction of the thickness of said first active semiconductor layer substantially changes broadly, and

said n-type thin film transistor has a second active semiconductor layer formed by doping its channel region with p-type impurities at a higher concentration than that in said first active semiconductor layer such that the concentration distribution in a direction of the thickness of said second active semiconductor layer has a peak near a surface.

30. A device according to claim 28, wherein each of said p- and n-type thin film transistors is formed such that the corresponding active semiconductor layer, a gate insulating film, and a gate electrode narrow down in this order, and provided with a source and a drain in said active semiconductor, said source and drain having LDD structures in accordance with the difference in width between said active semiconductor layer, said gate insulating film and said gate electrode.

31. A device according to claim 28, wherein a gate electrode is formed by patterning under a gate insulating film below the source and drain of each of

said thin film transistors.

32. An image display apparatus comprising:

an image display unit in which a plurality of pixels are arranged in a matrix;

a first control circuit for controlling the drive of rows of said image display unit; and

a second control circuit for controlling the drive of columns of said image display unit,

at least one of said image display unit and said first and second control circuits comprising CMOS transistors in each of which p- and n-type thin film transistors are formed and which have different operating voltages,

said p-type thin film transistor has a first active semiconductor layer formed by doping its channel region with p-type impurities such that the concentration distribution in a direction of the thickness of said first active semiconductor layer is substantially uniform, and

said n-type thin film transistor has a second active semiconductor layer formed by doping its channel region with p-type impurities at a higher concentration than that in said first active semiconductor layer such that the concentration distribution in a direction of the thickness of said second active semiconductor layer has a peak near a surface.

33. An image display apparatus comprising:

an image display unit in which a plurality of pixels are arranged in a matrix;

a first control circuit for controlling the drive of rows of said image display unit; and

a second control circuit for controlling the drive of columns of said image display unit,

at least one of said image display unit and said first and second control circuits comprising CMOS transistors in each of which p- and n-type thin film transistors are formed and which have different operating voltages,

said p-type thin film transistor has a first active semiconductor layer formed by doping its channel region with p-type impurities such that the concentration distribution in a direction of the thickness of said first active semiconductor layer substantially changes broadly, and

said n-type thin film transistor has a second active semiconductor layer formed by doping its channel region with p-type impurities at a higher concentration than that in said first active semiconductor layer such that the concentration distribution in a direction of the thickness of said second active semiconductor layer has a peak near a surface.

34. An apparatus according to claim 32, wherein the concentration of p-type impurities in said channel region of said p-type thin film transistor is

not more than 1 x $10^{18}/cm^3$.

35. An apparatus according to claim 32, wherein said image display unit has liquid crystal cells as said pixels and CMOS transistors with a high operating voltage, and

said first control circuit comprises a shift register having CMOS transistors with a relatively low operating voltage and an output buffer having CMOS transistors with a high operating voltage.